CLAIM LISTING

1. (original) A method for improved initialization of a high availability system that comprises a controller component and a plurality of peripheral components, the method comprising the steps of:

applying power by a controller component to a first peripheral component of the plurality of peripheral components;

when an indication that the first peripheral component has initialized is received by the controller component,

storing an identifier of the first peripheral component;

applying power by the controller component to a next peripheral component of the plurality of peripheral components that follows the first peripheral component in a power-up sequence;

when the first peripheral component, while initializing, locks up a bus that the controller component and the plurality of peripheral components share,

restarting the power-up sequence;

determining that an identifier of the first peripheral component was not stored; and

skipping the first peripheral component in the power-up sequence as a result of the step of determining to prevent the bus from being locked up.

2. (original) The method of claim 1 wherein the step of restarting comprises re-initializing the high availability system.

3. (original) The method of claim 2 further comprising the step of both expiring by a watchdog timer and triggering the re-initialization of the high availability system, when the first peripheral component locks up the bus.

4. (original) The method of claim 2 wherein the step of storing comprises storing the identifier in a memory device whose contents survive a re-initialization of the high availability system.

5. (original) The method of claim 4 wherein the memory device comprises a non-volatile random access memory.

6. (original) The method of claim 1 wherein the step of storing comprises storing a value in a location in a memory array that corresponds to the first peripheral component.

7. (original) The method of claim 6 further comprising the step of clearing the contents of the location in the memory array that corresponds to the first peripheral component prior to the step of applying power to the first peripheral component.

8. (original) A high availability system comprising:

a first peripheral;

a second peripheral, wherein the second peripheral follows the first peripheral in a power-up sequence;

a bus to which the first peripheral and the second peripheral are connected; and

a controller, connected to the bus, arranged to provide power to the first peripheral as part of the power-up sequence, arranged to store an identifier of the first peripheral and to apply power to the second peripheral when an indication that the first peripheral component has initialized is received, and arranged to restart the power-up sequence and skip the first peripheral in the power-up sequence as a result of determining that an identifier of the first peripheral was not stored when the first peripheral, while initializing, locks up the bus.

9. (original) The high availability system of claim 8 wherein restarting the power-up sequence comprises re-initializing the high availability system.

10. (original) The high availability system of claim 9 wherein the controller further comprises a clock that serves as a watchdog timer arranged to expire and trigger the re-initialization of the high availability system when the first peripheral component locks up the bus.

11. (original) The high availability system of claim 9 wherein the controller further comprises a memory device whose contents survive a re-initialization of the high availability system.

12. (original) The high availability system of claim 11 wherein the memory device comprises a non-volatile random access memory.

13. (original) The high availability system of claim 8 wherein the controller is further arranged to store a value in a location in a memory array that corresponds to the first peripheral serving as an identifier of the first peripheral.

14. (original) The high availability system of claim 13 wherein the controller is further arranged to clear the contents of the location in the memory array that corresponds to the first peripheral prior to the step of applying power to the first peripheral component.